International Journal of Gender, Science and Technology
..ISSN: 2040-0748

UGC Care Group I Journal
Vol-12 Issue-01 May 2023

A LOW POWER HIGH SPEED SENSE AMPLIFIER BASED FLIP-FLOP DESIGN IN 45nm MTCMOS

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Abstract— a flip-flop with a sensing amplifier that is appropriate for high-speed, low-power operation. The power and delay of the flip-flop are significantly decreased by the use of new sense-amplifier and single-ended latch stages. Through the use of MTCMOS optimization, the proposed SAFF can offer low voltage operation. The proposed SAFF has a shorter delay and less power than the current master-slave flip-flop (MSFF).The power-delay product of the suggested SAFF is better than that of the traditional SAFF and MSFF, and the proposed flip-flop's size is smaller. As a result, the proposed SAFF may operate reliably at low power supply voltages. But in this design, we're using 45nm technology, which enables us to deliver 1LVT (low threshold voltage) and still get the desired output. To achieve glitch- and contention-free functioning, the latch is subjected to a conditional cut-off method. Furthermore, by implementing MTCMOS optimisation, the proposed SAFF can offer low voltage operation.

Keywords— low-power; high-speed; flip-flop; sense-amplifier; MTCMOS

I.INTRODUCTION

A circuit that generates a stronger version of its input signal is referred to as an amplifier. However, since they are categorized based on their operational modes and circuit configurations, amplifier circuits are not all created equal. Small signal amplifiers are frequently used in "Electronics" because of their capacity to transform a relatively small input signal, such as one from a sensor like a camera, into a much larger output signal to power devices like relays, lamps, and loudspeakers. Electronic circuits can be classified as amplifiers in a variety of ways, ranging from operational amplifiers and small signal amplifiers to large signal and power amplifiers. The classification of an amplifier depends on the magnitude of the input signal, whether it is huge or little, the amplifier's physical setup, and how the input signal is processed, or how the input signal is related to the load's current flow.

Amplifiers can be conceptualized as a straightforward box or block containing the amplifying device, such as a bipolar transistor, field effect transistor, or operational amplifier, which has two input terminals and two output terminals (ground being common), with the output signal being significantly stronger than the input signal as it has been 'Amplified' Input resistance, also known as RIN, output resistance, or ROUT, and of course amplification, also known as Gain, or (A), are the three essential characteristics of an ideal signal amplifier. No matter how complex an amplifier circuit is, the relationship between these three features may still be demonstrated using a general amplifier model.

The Gain of the amplifier is the amplified difference between the input and output signals. Gain is a general term for the amount that an amplifier "amplifies" the input signal. For instance, the gain of the amplifier would be "50" if the input and output voltages were 1 volt and 50 volts, respectively. In other words, there has been a 50 percent increase in the input signal. This growth is known as gain. Simply dividing the output by the input results in amplifier gain. Since gain is a ratio, it has no units, but in electronics, it is frequently denoted by the letter "A" for amplification. Once this is determined, an amplifier's gain is simply calculated as "the output signal divided by the input signal."

The relationship between the signals measured at the output and the signal measured at the input is considered to be the introduction to amplifier gain. There are three types of amplifier gain that may be measured, and they are as follows: Examples of these various sorts of gains are provided below for voltage gain (Av), current gain (Ai), and power gain (AP), depending on the amount being measured.

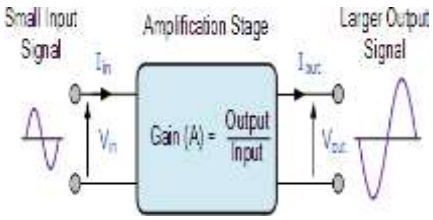


Fig 1. Amplifier gain

II. BACKGROUND

SENSE AMPLIFIER:

A sense amplifier is one of the components that makes up the circuitry on a semiconductor memory chip (integrated circuits) in current computer memory; the term itself dates

back to the time of magnetic core memory. The function of a sense amplifier, which is a component of the read circuitry required to read data from memory, is to sense. the low power signals from a bit line that correspond to a data bit (1 or 0) stored in a memory cell and amplifying the small voltage swing to understandable logic levels so the data may be appropriately understood by logic outside the memory. Early sense amplifiers for core memory occasionally included as many as 13 transistors, whereas modern sense-amplifier circuits typically have two to six (often four) transistors. There are typically hundreds or thousands of identical sense amplifiers on a modern memory chip since there is one sense amplifier for every column of memory cells. As a result, one of the only analogue circuits in a computer is the sense amplifier.

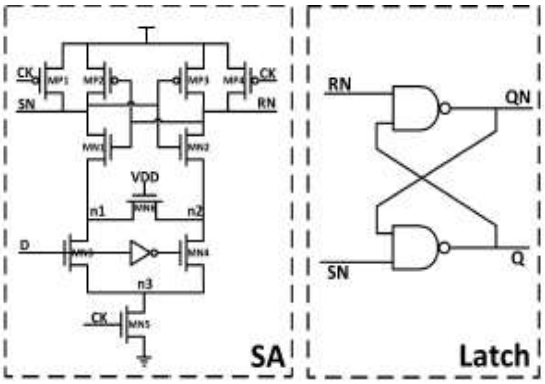
FLIP-FLOP:

A flip-flop is a fundamental component of a digital memory circuit that stores one bit of data. Flip-flops are the fundamental blocks of most sequential circuits. It is also referred to as a binary or one-bit memory or a bi stable multivibrator. In sequential circuits, flip-flops are utilised as memory components. The output is obtained in a sequential circuit from combinational circuit or flip-flop or both. The state of the flip-flop changes while the clock pulse is active and is unaffected when it is not. In specifically, clocked flip-flops and unlocked flip-flops (also known as latches) are used as memory components in synchronous sequential circuits and asynchronous sequential circuits, respectively.

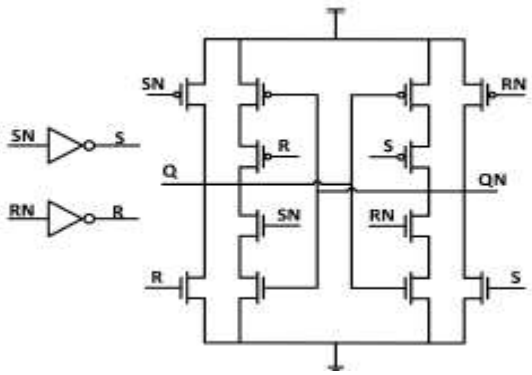
• A flip-flop is a gadget that may be used, and it has two stable states that are denoted as 0 and 1.
• It verifies the inputs, but only when a clock signal or other control signal specifies a change in the output.
• They can be categorised as synchronous or asynchronous flip-flops.
• It serves as the foundation for many sequential circuits, including counters.
• Flip-flops always display a time signal.
• Flip-flop can be built from Latches
• Example: D Flip-flop, JK Flip-flop

III. CONVENTIONAL SENSE AMPLIFIER BASED FLIPFLOP:

The set reset (S-R) latch and SA components of the traditional SAFF are shown in the diagram. Here is how the SAFF runs. While CK is low, the voltage of SN and RN is pre-charged to VDD, and the latch maintains the output data. The pre-charge transistors MP1 and MP4 are turned off, while MN5 is turned on, at the rising edge of CK. Depending on the input data, one of the pre-charge nodes (SN and RN) is drained to 0 while the other stays VDD. The latch then records the fresh data from the SA stage. When CK is high, the SA's output is maintained by the transistor MN6 that is constantly on. For instance, SN must be kept at 0 during CK's positive half cycle since it is discharged to 0 in response to D = 1 at the rising edge of CK. D might turn to 0 during the positive half cycle, therefore SN should have another path to 0 available at this time. MN6 also functions at this time. The main issues with the standard SAFF are the enormous power of the pre-charge operation and the imbalanced delay of the S-R latch. Additionally, the always-on transistor reduces the SAFF at low supply voltages' robustness.

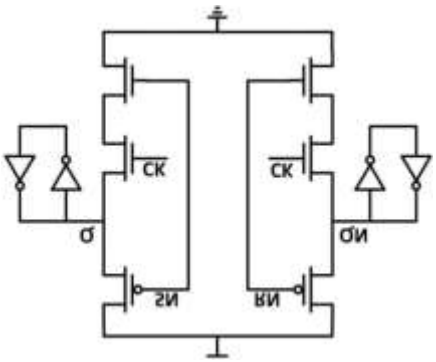


(**A**) Schematic of the conventional sense-amplifier-based flip-flop

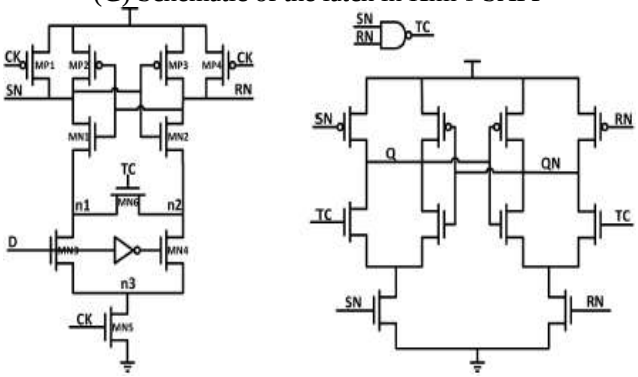


(**B**) Schematic of the latch in Nikolic's SAFF.

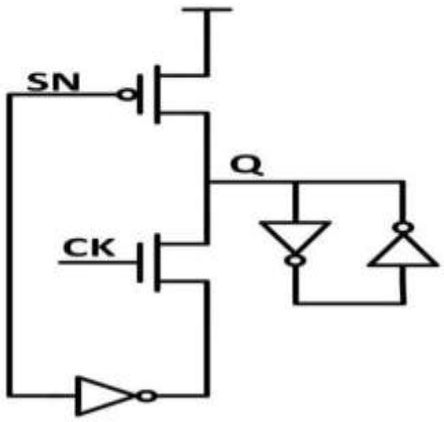
In order to reduce the latency of the SAFF, Nikolic et al. devised a latch for the SAFF that consisted of two inverters and numerous complicated logics to eliminate the delay dependence between Q and QN in the standard SAFF. Figure 2b depicts the latch's schematic. The four signals SN, RN, S, and R are directly formed from the output Q and QN after the two inverters are used to invert the SN and RN. The CK-to-Q delay is shortened and the reliance between Q and QN is eliminated. The optimization of the delay in this manner may not fulfill the expectations since it is impossible to ignore the delay of the inverters and sophisticated logic.



(**C**) Schematic of the latch in Kim's SAFF



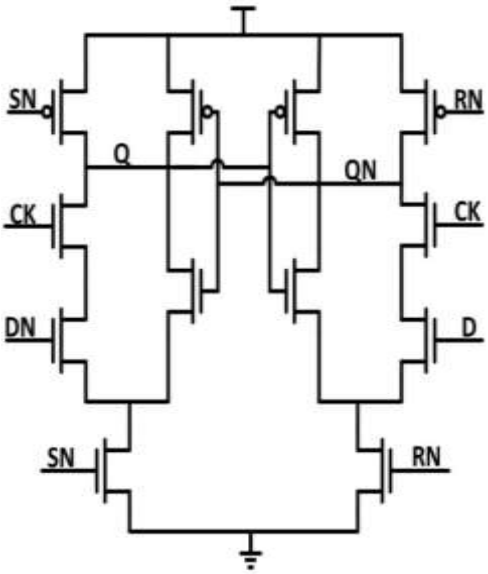
(**D**) Schematic of the latch in Jeong's SAFF



(**E**) Schematic of the latch in Lin'Ssaff

(**F**) Schematic of the latch in Strollo's SAFF

According to Figure A, Kim et al. presented a SAFF with a latch made up of two N-C2MOS circuits and two pairs of inverters. The latch was developed by Lin et al. into a single-ended structure, which significantly decreased power consumption. By making the latch a single-ended structure, Lin et al. significantly decreased the power usage. Figure E depicts the latch's schematic for Lin's SAFF. Since there are few logics between SN and the output Q, this type of SAFF has a much shorter latency than a normal SAFF. However, there is a significant malfunction that will boost the SAFF's power consumption while the output Q and the next data



input are both at high levels. Additionally, power consumption will rise as a result of the back-to-back inverters' current conflict. Kim's SAFF was merged with the standard SAFF in Strolloetal's proposal to create a SAFF that operated quickly and flawlessly. Figure depicts the schematic for the latch in Strollo's SAFF.

Due to the always-on transistor in the SA stage, the voltage operation issue affects all of the SAFF mentioned above. The SAFF uses a detecting signal to gate the always-on transistor in order to solve this issue and get around the current contention of earlier SAFFs. Figure 3.6 displays Jeong's SAFF's schematic. The detection signal is converted from the control signal of the SA stage's always-on transistor. The fundamental issue with Jeong's SAFF is that the logic for transition completion detection will prolong the FF's propagation latency.

DISADVANTAGES

All of the SAFFs mentioned above experience low voltage functioning issues as a result of the SA stage's always-on transistor. Power consumption will also rise as a result of the back-to-back inverters' current contention.

IV. PRAPOSED METHOD

Figure 2 depicts the planned SAFF's schematic. Similar to earlier SAFFs, the SAFF is made up of a SA stage and a slave latch, as shown in Figure 2. According to earlier parts, the SA stage might record data immediately following CK's rising edge and apply the slave latch to keep the output stable throughout CK's negative half-cycle.

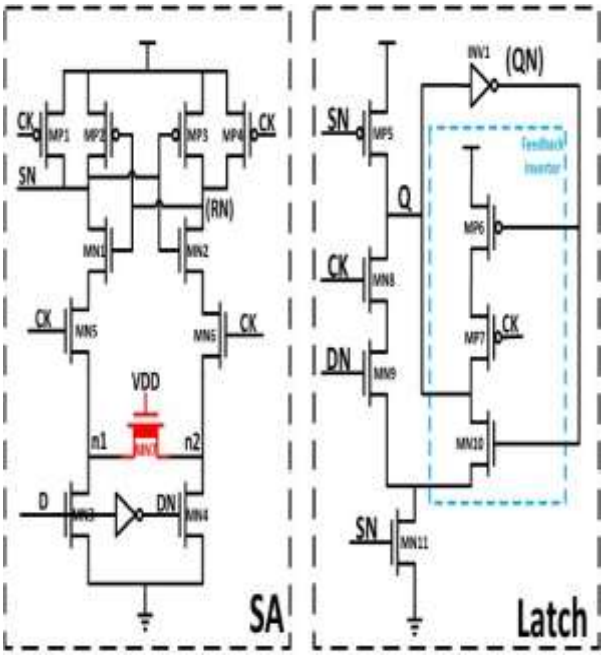


Figure: Schematic of the proposed SAFF.

Even if some internal nodes, including n1, n2, and n3 in Figure 2a, are discharged to the VSS during the data-capturing operation regardless of the input data, the SA stage in the conventional SAFF must charge all of the internal nodes during pre-charge operation. In reality, the pre-charge operation of n1, n2, and n3 is a waste of electricity and has no real impact on how the SA works.Since the voltages of nodes 1, 2, and 3 are charged close to the power supply voltage during pre-charge operation and transistors MN3 and MN4's sizes are big to reduce propagation delay, the pre-charge operation of these nodes represents a significant energy waste.

The NMOS controlled by CK (MN5) in this project is split in two (shown as MN5 and MN6 in Figure 2) and relocated. Since the transistors MN5 and MN6 are off when CK is low thanks to the conversion, the nodes connected to MN3 and MN4 are no longer required to charge during pre-charge operation. Throughout the procedure, the voltages of n1 and n2 in Figure 4.1 are low. As a result, the pre-charge operation's power is significantly decreased. Pre-charge power is an essential component of the SAFF's power consumption, therefore the proposed SAFF's power consumption can be significantly lowered.

The hold time of the suggested SAFF can be enhanced by the proposed SA structure. At the leading edge of CK, the new SA stage can capture the input data more quickly. This is primarily due to the internal nodes n1 and n2 staying low during the procedure and having a shorter discharge time. As a result, the proposed SAFF's hold time is shortened. The setup time of the proposed SAFF increases slightly as quicker data capturing does, but only little because to the fast internal node discharge time.

The planned SAFF uses a new single-ended latch. The suggested latch combines Lin's and Strollo's latch benefits for quick and energy-efficient operation.To achieve glitch-free operation, the latch in Figure 4.1's initial stage is comparable to Strollo's latch. Lin's latch flaw has been completely fixed. This is primarily because MN9 was inserted. The pull-down path is entirely blocked by MN9 when D is high, DN is low, and DN is low. As a result, the bug is fixed. To get around the existing issue, back-to-back inverters that are utilized for data storage have been updated. The feedback inverter is switched off by MN11 for the output Q to transition from low to high, indicating that the voltage of the SN is low.

Similar to this, MP7 disables the feedback inverter when the output Q changes from high to low. As a result, the feedback inverter's influence on the output transition is entirely removed. The size of the transistors associated to RN generation in the SA stage might be decreased because the latch has nothing to do with RN, which would minimize power consumption. When appropriate, the latch's inverterINV1 could produce complementary output QN, and the time difference between Q and QN is the same as an inverter delay (MSFF).

At low supply voltages, the always-on transistor causes function failures as indicated. Although the detection logic effectively resolves low voltage function failures, the complicated logic lengthens the time and uses more energy. In order to solve the issue, MTCMOS optimisation is used in this paper. The driving capability of the always-on transistor should be less than that of the pull-down transistors in order to prevent low voltage function failures.

The SAFF experiences function failures when the driving capacity of two stacked LVT-NMOSs and the always-on transistor increases beyond that of two stacked LVT-NMOSs owing to technical variation. Three LVT-NMOSs are stacked when an LVT-NMOS is used as the always-on transistor. At low supply voltages, function failures can occur because the current of three stacked LVT-NMOSs can be greater than that of two stacked LVT-NMOSs (I1 / I2 1).

Since the current of two stacked LVT-NMOSs and one HVT-NMOS is always smaller than that of two stacked LVT-NMOSs (I1 / I3 > 1 all the time), function failures stop happening when the always-on transistor is switched to an HVT-NMOS. In order to assure proper operation, the current of the always-on transistor and the two stacked LVT-NMOSs must be greater than the leakage current. The requirement is still met when an HVT-NMOS always-on transistor is used. Therefore, multi-threshold optimisation can effectively address the issue of low voltage function failures. As seen in Figure 2, the always-on transistor in the proposed design has a high threshold whereas the others have a low threshold.

COMPARISION OF ALL METHODS

Table1 Comparison Of Different Circuits

Name	Power consumption(mw)	Time delay(ns)	Number of Transistors required
EXISTING METHOD	2.64	55	28
NIKOLIC'SSAFF	7.301	30	28
LIN'SSAFF	7.11	0.3	20
STROLLO'SSAFF	6.24	30	24
JEONG'SSAFF	8.39	40	26
PROPOSED METHOD	0.04	0.43	22

V. CONCLUSION

In this paper, a low-power, high-speed SAFF is suggested. The SA stage's structure is intended to use 45nm technology in order to reduce the SAFF's pre-charge power. A single-ended latch that is glitch- and contention-free is also suggested. The SAFF's delay and power are considerably enhanced by the use of the new SA stage and single-ended latch. The proposed improvement's power-delay product in comparison to the traditional SAFF. The proposed SAFF is a good option for replacing MSFFs in digital systems in order to enable low-power, high-speed operation due to the enhancement over the MSFF. Furthermore, by implementing MTCMOS optimization, the suggested SAFF can offer low voltage operation.

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